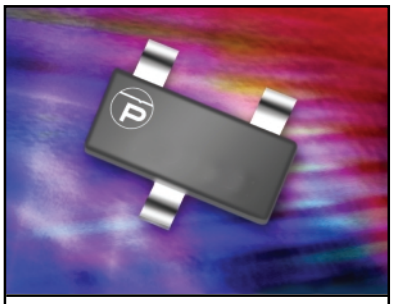
PSOT03LC thru PSOT36LC

Only One Name Means ProTek'Tion™

ULTRA LOW CAPACITANCE TVS ARRAY

APPLICATIONS



SOT-23

- ✔ Ethernet - 10/100 Base T
- ✔ Cellular Phones
- ✔ FireWire
- ✔ Audio/Video Inputs
- ✔ Portable Electronics

IEC COMPATIBILITY (EN61000-4)

- ✔ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✔ 61000-4-4 (EFT): 40A - 5/50ns
- ✔ 61000-4-5 (Surge): 12A, 8/20µs - Level 1(Line-Ground) & Level 2(Line-Line)

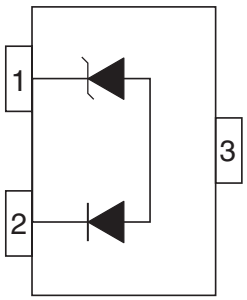
FEATURES

- ✔ ESD Protection > 40 kilovolts
- ✔ 500 Watts Peak Pulse Power per Line (tp = 8/20µs)
- ✔ Low Clamping Voltage
- ✔ Available in Multiple Voltage Types Ranging from 3V to 36V
- ✔ ***ULTRA LOW CAPACITANCE: 5pF***

MECHANICAL CHARACTERISTICS

- ✔ Molded JEDEC SOT-23
- ✔ Weight 14 milligrams (Approximate)
- ✔ Flammability rating UL 94V-0
- ✔ 8mm Tape and Reel Per EIA Standard 481
- ✔ Device Marking: Marking Code

PIN CONFIGURATION



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DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power - t_p = 8/20µs (See Figure 1)	P_{PP}	500	W
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE (See Note 2) @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I_P = 1A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @8/20µs V_C @ I_{PP}	MAXIMUM LEAKAGE CURRENT @V_{WM} I_D µA	TYPICAL CAPACITANCE @0V, 1 MHz C pF
PSOT03LC	03L	3.3	4.0	7.0	10.9V @ 43.0A	125	5
PSOT05LC	05L	5.0	6.0	9.8	13.5V @ 42.0A	20	5
PSOT08LC	08L	8.0	8.5	13.4	16.9V @ 34.0A	10	5
PSOT12LC	12L	12.0	13.3	19.0	25.9V @ 21.0A	1	5
PSOT15LC	15L	15.0	16.7	24.0	30.0V @ 17.0A	1	5
PSOT24LC	24L	24.0	26.7	43.0	49.0V @ 12.0A	1	5
PSOT36LC	36L	36.0	40.0	51.0	76.8V @ 9.0A	1	5

Note 1: Positive potential is applied from pin 1 to 2; pin 2 is ground.
Note 2: Do not test or surge from pin 2 to 1. PIV typically greater than 100V for the rectifier diode.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

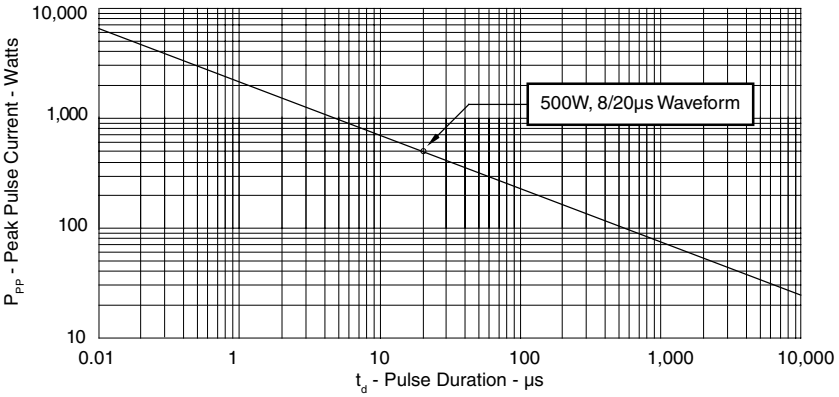
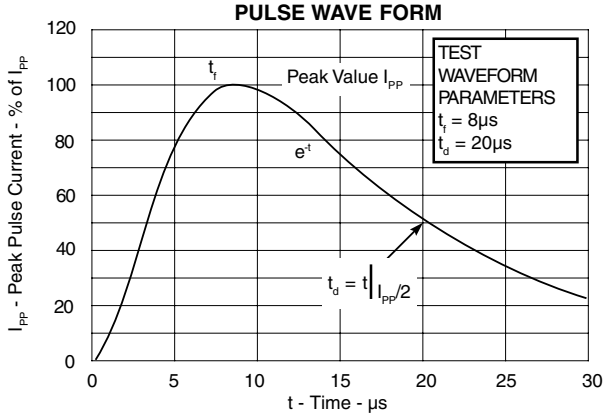


FIGURE 2
PULSE WAVE FORM



GRAPHS

FIGURE 3
POWER DERATING CURVE

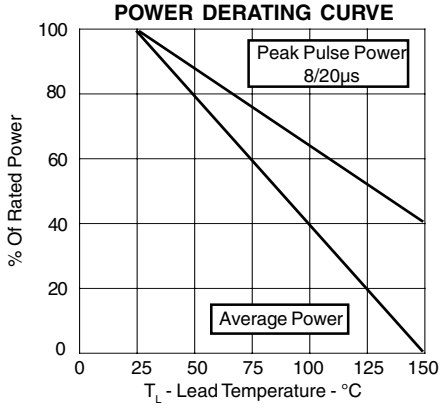
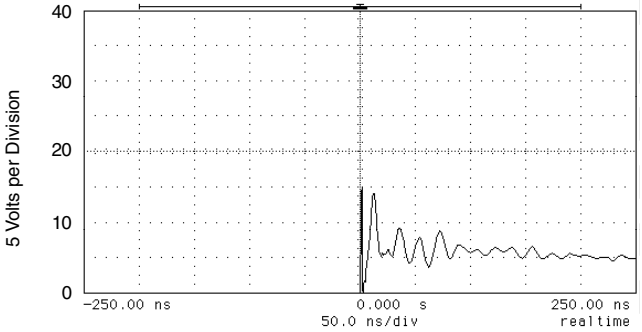
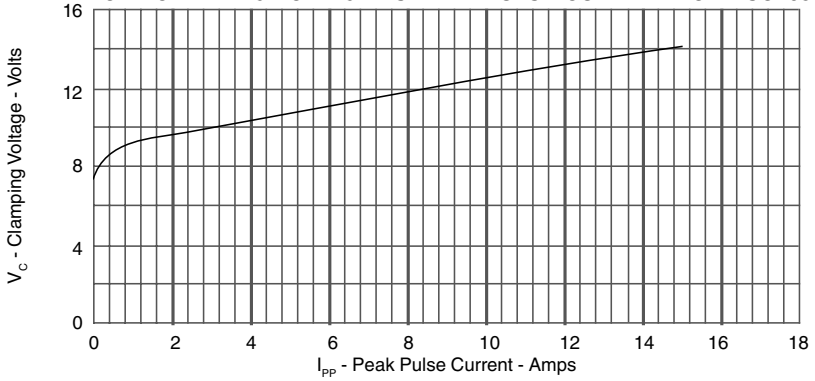


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR PSOT03LC



ESD Test Pulse: 7 kilovolt, 1/30ns (waveform)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT FOR PSOT05LC



PSOT03LC thru PSOT36LC

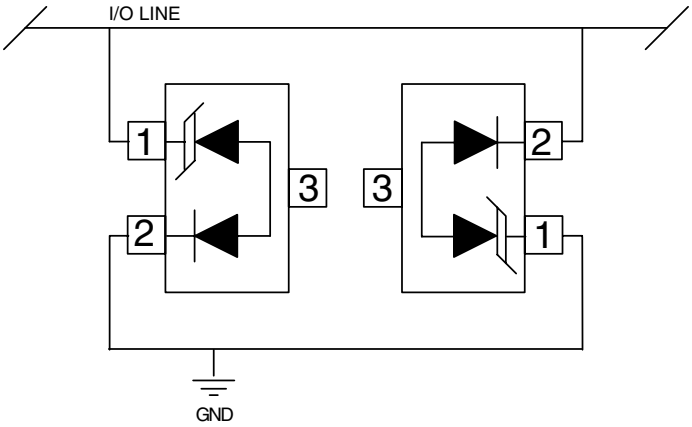
APPLICATION NOTE

The PSOTxxLC Series are low capacitance TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product series provides unidirectional & bidirectional protection, with a surge capability of 500 Watts P_{PP} per line for an 8/20µs waveform and ESD protection > 40 kilovolts.

BIDIRECTIONAL COMMON-MODE CONFIGRUATION (Figure 1)

Two PSOTxxLC devices, when used in paralell, provide protection in a common-mode configuration as depicted in Figure 1.

Figure 1 - Common-Mode I/O Port Protection



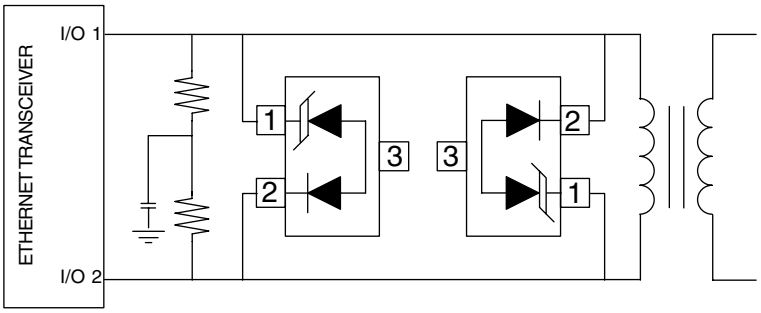
Circuit connectivity is as follows:

- ✔ I/O Line is connected to Device 1, Pin 1.
- ✔ I/O Line is connect to Device 2, Pin 2.
- ✔ Device 1, Pin 2 is connected to ground.
- ✔ Device 2, Pin 1 is connected to ground.
- ✔ Device 1 & 2, Pin 3 is not connected.

BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGRUATION (Figure 1)

In addition, two PSOTxxLC devices, when used in paralell, provide protection in a differential-mode configuration for Ethernet applications as depicted in Figure 2.

Figure 2 - Differential-Mode Ethernet Protection



Circuit connectivity is as follows:

- ✔ I/O Line 1 is connected to Device 1, Pin 1.
- ✔ I/O Line 1 is connect to Device 2, Pin 2.
- ✔ I/O Line 2 is connected to Device 1, Pin 1.
- ✔ I/O Line 2 is connect to Device 2, Pin 2.
- ✔ Device 1 & 2, Pin 3 is not connected.

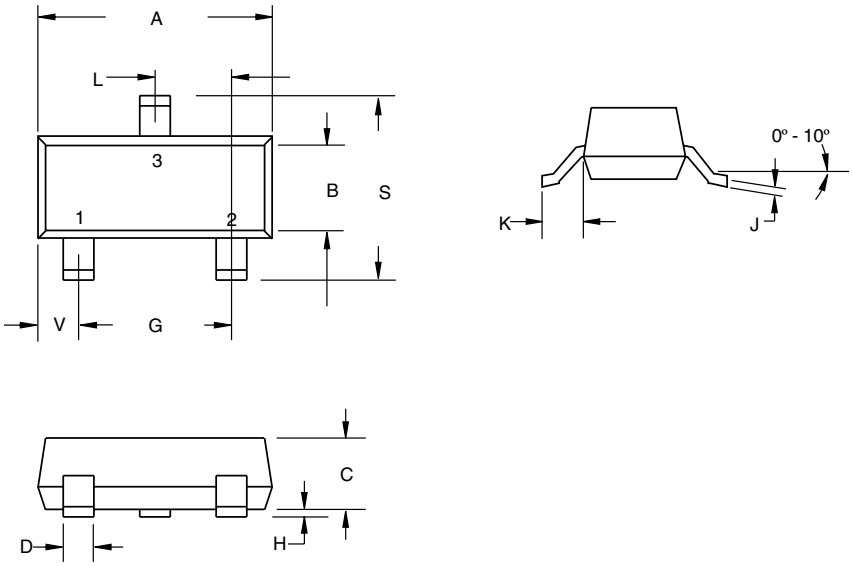
CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✔ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✔ The path length between the TVS device and the protected line should be minimized.
- ✔ All conductive loops including power and ground loops should be minimized.
- ✔ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✔ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE

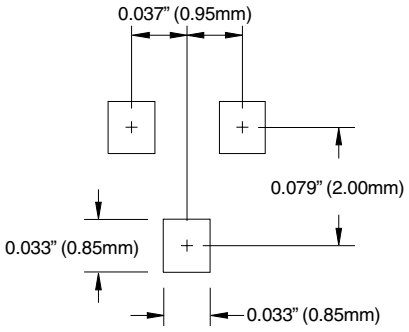


SOT-23

PACKAGE DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

MOUNTING PAD



NOTES

1. Dimensioning and tolerances per ANSI Y14.5M, 1985.
2. Controlling Dimension: Inches
3. Pin 3 is the cathode (Unidirectional Only).
4. Dimensions are exclusive of mold flash and metal burrs.

TAPE & REEL ORDERING NOMENCLATURE

1. Surface mount product is taped and reeled in accordance with EIA-481.
2. Suffix -T7 = 7 Inch Reel - 3,000 pieces per 8mm tape, i.e., *PSOT05LC-T7*.
3. Suffix -T13 = 13 Inch Reel - 10,000 pieces per 8mm tape, i.e., *PSOT05LC-T13*.

Outline & Dimensions: Rev 1 - 11/01, 06012